REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

By this amendment Claims 1 and 2 have been amended to recite more specific features of the invention and Claim 7 amended to provide clear antecedent basis.

Amended independent Claim 1 recites a microprocessor built on a semiconductor chip including, *inter alia*, a clock generating circuit, coupled to the central processing unit, adapted to generate a plurality of clock signals including a first clock signal, a second clock signal and an internal clock signal. A clock switching control circuit is adapted to control an operation to switch a synchronous clock signal providing one of the first clock signal and the second clock signal to the external bus interface control circuit in accordance with the external device select signal. A first clock terminal is adapted to supply the first clock signal to a first external device which is to be coupled to the microprocessor and a second clock terminal is adapted to supply the second clock signal to a second external device which is to be coupled to the microprocessor. The clock generating circuit provides the internal clock signal to the central processing unit, the second clock signal has a different frequency from the first clock signal, and the first and second clock signals are output from the

microprocessor to the first and second external devices, respectively, in parallel.

Independent Claim 2 recites that the clock pulse generator generates the first clock signal, the second clock signal and an internal clock signal. The first clock signal has a predetermined frequency different from that of the second clock signal, and the clock pulse generator provides the internal clock signal to the central processing unit. The microprocessor includes first and second external clock output terminals outputting the first and second clock signals, respectively, in parallel.

While Kakiage is directed toward a bus controller and information processing device, Kakiage does not teach or suggest the above combination of features found in independent Claims 1 or 2. For example, independent Claims 1 and 2 recite that the clock generating circuit and the clock pulse generator, respectively, generate the first clock signal, the second clock signal and the internal clock signal and that the first and second clock signals are output in parallel.

As can be seen from Fig. 1 of Kakiage, the external clock signal 100 is supplied directly to the frequency synthesizer 4, the external device 21 and the external access controlling signal generator 8. Not only does Kakiage not generate the first, second and internal clock signals as recited in the independent claims, but Kakiage

also does not teach or suggest that the first and second clock signals are output in parallel. Moreover, Kakiage does not disclose that the second clock signal has a different frequency from said first clock signal as recited in independent Claim 1 nor that the first clock signal has a predetermined frequency different from that of the second clock signal as recited in independent Claim 2.

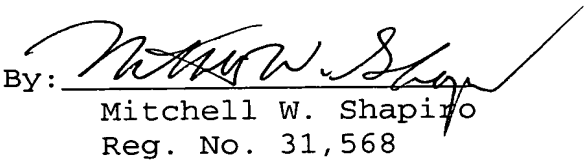
In that Yanagiuchi fails to overcome these deficiencies, independent Claims 1 and 2, and the claims that depend therefrom, are distinguishable from the cited references.

The application is therefore in condition for allowance. An early Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and

has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 
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June 15, 2005